1992

An analytical model for LDD MOS transistors in the breakdown mode

Zbigniew A. Kozlowski
Lehigh University

AUTHOR:

Kozlowski, Zbigniew A.

TITLE:

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DATE: May 31, 1992

AN ANALYTICAL MODEL FOR LDD MOS TRANSISTORS IN THE BREAKDOWN MODE

by

Zbigniew A. Kozlowski

A Thesis
Presented to the Graduate Committee
of Lehigh University
in candidacy for the degree of
Master of Science
in Electrical Engineering

Lehigh University

1992

Certificate of Approval

This thesis is accepted and approved in partial fulfillment of the requirements for the degree of Master of Science

May 14, 1992
(date)

Professor in Charge

Chairman of Department

Acknowledgments

I would like to thank my advisor Dr. Marvin White for his guidance and assistance on this project. I would also like to thank Yin Hu at Lehigh University for helpfull discussions concerning the electric field model in LDD structures. Finally, I would like to extend my thanks to Charles Pearce at AT&T Microelectronics for introducing me to the subject of the snap-back breakdown in MOS transistors.

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ABSTRACT

The purpose of this thesis is to develop an analytical breakdown model for LDD (Lightly Doped Drain) MOS transistors operating in the breakdown region. The model is based on the previously published models, i.e. the model for the source-drain breakdown in conventional short-channel transistors and the lateral channel electric field model in LDD structures. It predicts the current-voltage characteristics up into the breakdown region, as well as the breakdown voltage.

The theory is verified by comparing the calculated against the measured I-V characteristics for a n-channel LDD MOS transistor fabricated in 1.25 μm CMOS technology. Good agreement is found between theory and experiment. In the worst case, i.e for the gate bias eqaual to 4 V, the deviation of the calculated value of the drain current from the measured value is 13 percent and occurs in the saturation region. The breakdown voltages agree within 0.4 V.

The model is implemented in a computer program written in Quick Basic and run on IBM compatible Personal Computers.

CHAPTER 1

1. Introduction

1.1 Historical Review

In long channel MOS transistors, i.e. transistors with channel lengths on the order of 10 μm and greater, the I-V characteristic in the breakdown region is typical of a p-n junction avalanche breakdown. As the channel length decreases, the I-V characteristic of a n-channel transistor exhibits a negative resistance or a snap-back phenomenon (Fig. 1.1). When snap-back occurs, the sustaining voltage is lower than the voltage needed to initiate the breakdown. Another phenomenon, characteristic of short-channel transistors, is the dependance of breakdown voltage on the channel length i.e. breakdown voltage decreases with decreasing channel length.

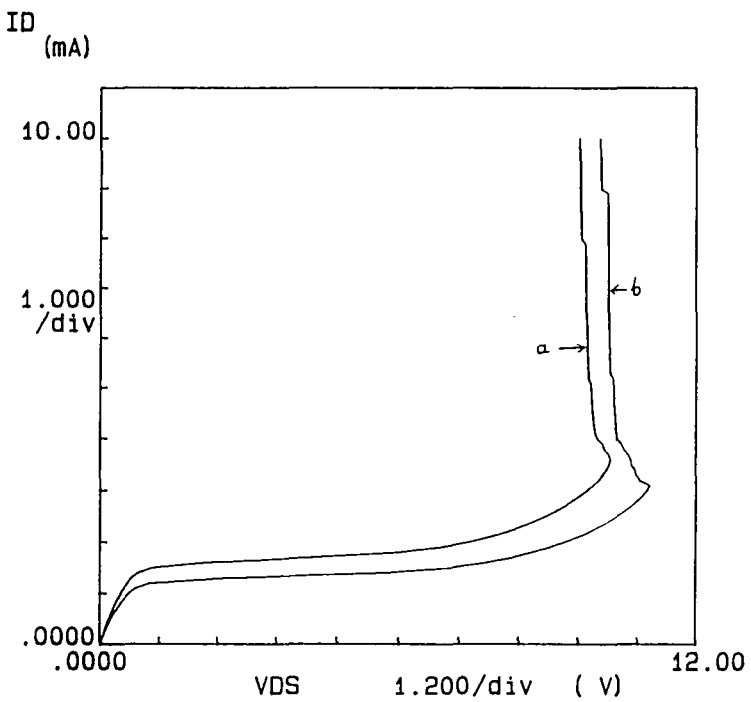

Fig. 1.1 Source-drain breakdown characteristics of a short channel n-MOS transistor: (a) $L_{eff} = 1\ \mu m$, (b) $L_{eff} = 1.25\ \mu m$

Several authors have studied the "snap-back" breakdown mechanism in short-channel n-MOSFETs. Kennedy et al. [1] was the first who suggested that a positive feedback effect involving parasitic bipolar transistor action is the main breakdown mechanism. Toyabe et al. [2] using two-dimensional numerical calculations concluded that the voltage drop $R_B I_B$ resulting from the flow of the substrate current I_B through the substrate spreading resistance R_B acts as a positive back-gate bias that increases the channel current and, subsequently, I_B (eq. 2.4). This positive feedback of the self-back-biasing continues until the source-substrate junction is turned-on injecting electrons into the substrate which occurs when $R_B I_B \approx 0.65\,V$.

Sun et al. [3] showed that turning-on of the source junction is not a sufficient condition for the drain-source breakdown, and that breakdown occurs at a higher source-drain voltage than the one corresponding to the turn-on of the source junction. From the condition $\alpha_0 M = 1$ for the common-emitter breakdown of the bipolar transistor, and the following expressions for the common-base current gain α_0 and the avalanche multiplication factor M:

$$\alpha_0 = sech\left(\frac{L_{eff}}{L_D}\right) \approx 1 - \frac{1}{2}\left(\frac{L_{eff}}{L_D}\right)^2 \tag{1.1}$$

$$M = \frac{1}{1 - (BV_{CE0}/BV_{CB0})^n} \tag{1.2}$$

Sun derived an expression for the breakdown voltage of the short-channel MOS transistor:

$$BV_{DS} = BV_{CE0} \approx \left(\frac{L_{eff}^2}{2L_D^2}\right)^{\frac{1}{n}} BV_{CB0} \tag{1.3}$$

where BV_{CE0} is the common-emitter breakdown voltage of the parasitic n-

p-n transistor formed by the source (emitter), the substrate (base), and the drain (collector) region; BV_{CB0} is the common-base breakdown voltage (or drain-substrate junction breakdown voltage); L_{eff} is the effective channel length (or the base width); L_D is the electron diffusion length in the base, and n is the empirical constant (usually between 4 and 6). Equation (1.3) shows the dependance of the breakdown voltage on the transistor's channel length.

The most general analytical breakdown model for short channel MOSFET transistors was proposed by Hsu et al. [4,5]. He showed that two conditions have to be satisfied before source-drain breakdown can occur:

1. The source-substrate junction has to be turned on
2. The multiplication factor has to be large enough to cause a significant positive feedback effect.

When the substrate resistance is small and/or the gate voltage is low (small channel current) the first condition determines the breakdown voltage, as was the case in Toyabe's work. On the other hand, when the substrate resistance is high (also, when an external resistor is connected to the substrate terminal), and/or when the gate voltage is high then the source-substrate junction becomes turned-on at lower drain voltage. However, the breakdown does not occur until the second condition is met which requires higher drain voltage. This was also observed by Sun.

1.2 Source of Thesis

The purpose of this thesis is to extend the analytical breakdown model proposed by Hsu to LDD (Lightly Doped Drain) MOS transistors. The LDD structures [6,7] were developed for MOS transistors with channel lengths

below 1.5 μm in order to decrease the lateral electric field in the channel in the vicinity of the drain and as a result to reduce hot-carrier effects.

One of these effects is generation of hole-electron pairs resulting from the impact ionization of the channel current carriers in the high field region near the drain. The generated holes flow to the substrate giving rise to a substrate current, which is responsible for the lowering of the source-drain breakdown voltage. The electrons are swept to the drain increasing the total drain current.

In order to predict the breakdown voltage as well as to calculate theoretical I-V characteristics in the breakdown region it is necessary to know the value of the avalanche multiplication factor M of the carriers in the channel which is a strong function of the lateral electric field. The multiplication factor can be expressed as:

$$M = \frac{1}{1 - S} \tag{1.4}$$

where S is the ionization integral given by [8]

$$S = \int_{-L_{sat}}^{y_d} \alpha(E_y)\ dy \tag{1.5}$$

and

$$\alpha(E_y) = A_i \exp\left(- \frac{B_i}{E_y(y)} \right) \tag{1.6}$$

is the ionization rate, A_i and B_i are the ionization parameters, E_y is the lateral electric field in the channel. The integration in (1.5) is carried out over the length of the saturation region that extends from the pinch-off point $-L_{sat}$ to the edge of the depleted region y_d as shown in Fig. 3.3.

Ko et al. [9] developed an expression for the lateral electic field in conventional, non-LDD transistors:

$$E_y = \sqrt{A^2 [\, V(y) - V_{Dsat} \,]^2 + E_{sat}^2} \tag{1.7}$$

where V_{Dsat} is the saturation voltage, E_{sat} is the electric field at the pinch-off point, and A is the parameter related to the drain junction depth, the oxide thickness, the source-drain voltage and the substrate doping concentration. Using the expression for E_y in (1.6), together with (1.4) and (1.5) Ko derived an expression for the avalanche multiplication factor M:

$$M = \left[1 - \left(\frac{A_i}{A} \right) \left(\frac{E_{ymax}}{B_i} \exp\left(- \frac{B_i}{E_{ymax}} \right) \right) \right]^{-1} \tag{1.8}$$

where E_{ymax} is the maximum electric field near the drain. This expression for M was used by Hsu in his breakdown model for conventional MOS transistors.

For LDD transistors which are the subject of this thesis the multiplication factor is calculated numerically using equations (1.4) through (1.6). A profile of the lateral electric field $E_y(y)$ and the length of the saturation region L_{sat} are calculated by a computer program which implements an analytical model for lateral electric field in LDD structures developed by Hu et al. [10]. Both models, i.e. the breakdown and the electric field model are verified by comparing the calculated I-V curves with the measured ones.

CHAPTER 2

2. Theory of Source-Drain Breakdown in Short-Channel n-MOSFETs

2.1 Physical Mechanism

When the lateral electric field near the drain is large enough, the carriers (electrons in a n-channel transistor) have enough energy to generate hole-electron pairs by impact ionization. The electrons generated this way are swept into the drain, while the holes flow first towards the source and then into the substrate [11] as shown in Fig. 2.1.

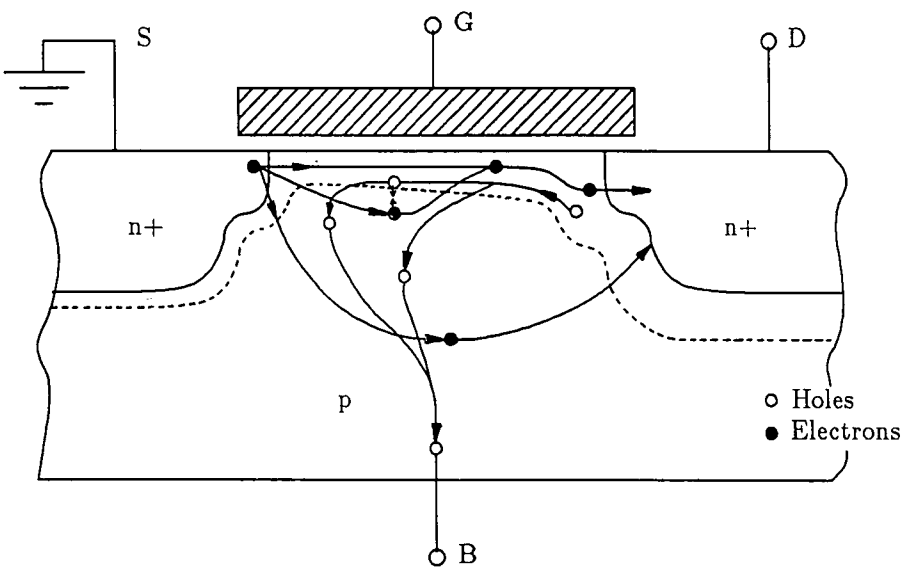

Fig. 2.1. Schematic diagram showing flow of holes and electrons after source-drain breakdown.

This hole current develops a voltage drop across the substrate spreading resistance which acts as a positive back-gate bias decreasing the threshold voltage and increasing the channel current [2]. Additionally, this ohmic drop

tends to forward bias the source-substrate junction. As soon as the potential in the vicinity of the source builds up to about 0.65 V the junction will be turned-on injecting electrons from the source (emitter) to the substrate (base) of the parasitic n-p-n bipolar transistor. Most of these injected electrons are then collected by the drain (collector) increasing the total drain current and avalanche-generating additional holes. The hole current flows through the substrate raising potential near the source even higher and causing more electron injection. As the loop gain of this positive feedback approaches 1, the drain current rapidly increases which results in source-drain breakdown. Some of the injected electrons may recombine with the hole current as shown schematically in Fig. 2.1.

The electric field in the substrate is in such a direction [11] that most of the electrons injected out of the source junction are pushed towards the channel increasing the negative charge density next to the drain. This results in higher electric field which in turn raises the avalanche multiplication factor above its value without electron injection. Thus, a lower drain-to-source bias is sufficient to sustain the same drain current level. These phenomena are responsible for the observed negative resistance.

A fraction of the injected electrons travel along semi-circular trajectories [2] and enter the drain below the high field region. These electrons do not generate additional hole-electron pairs but they do contribute to the total drain current.

2.2 Analytical Model

As soon as the hole current starts to flow into the substrate (i.e. when $M>1$) the voltage drop $I_B R_B$ increases the potential next to the source, forward

biasing the source-substrate junction. Including the series resistance of the source R_S and an optional external back-gate bias V_{SB}, this forward-bias voltage can be written as (Fig. 2.2)

$$V_F = I_B R_B - I_S R_S - V_{SB} \tag{2.1}$$

where

R_B is the substrate spreading resistance

R_S is the series resistance of the source

I_B is the substrate current

I_S is the source current

V_{SB} is the external back-gate bias

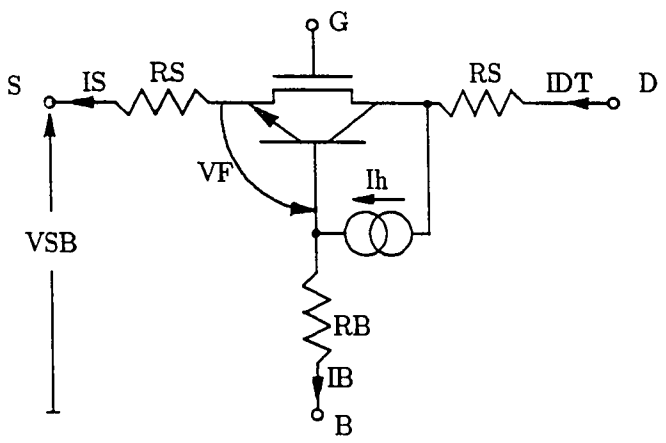

Fig. 2.2. Equivalent circuit of a short-channel MOS transistor.

When $V_F < 0.65$ V, that is when the source-substrate junction is turned-off, the source current I_S, the total drain current I_{DT}, and the substrate current I_B can be expressed as

$$I_S = I_{ch} \tag{2.2}$$

$$I_{DT} = M I_{ch} \tag{2.3}$$

$$I_B = I_{DT} - I_S = (M - 1) I_{ch} \tag{2.4}$$

where I_{ch} is the channel current of the MOS transistor, and M is the avalanche multiplication factor.

When V_F reaches about 0.65 V, the turn-on voltage of the parasistic n-p-n transistor, the source begins to inject electrons into the substrate (base) giving rise to an injection current I_e that can be expressed as:

$$I_e = I_0 [\exp(V_F/V_t) - 1] \tag{2.5}$$

where

I_0 is the reverse saturation current of the source junction

$V_t = kT/q$ is the thermal voltage.

Now the source current I_S is equal to (Fig. 2.3)

$$I_S = I_e + I_{ch} \tag{2.6}$$

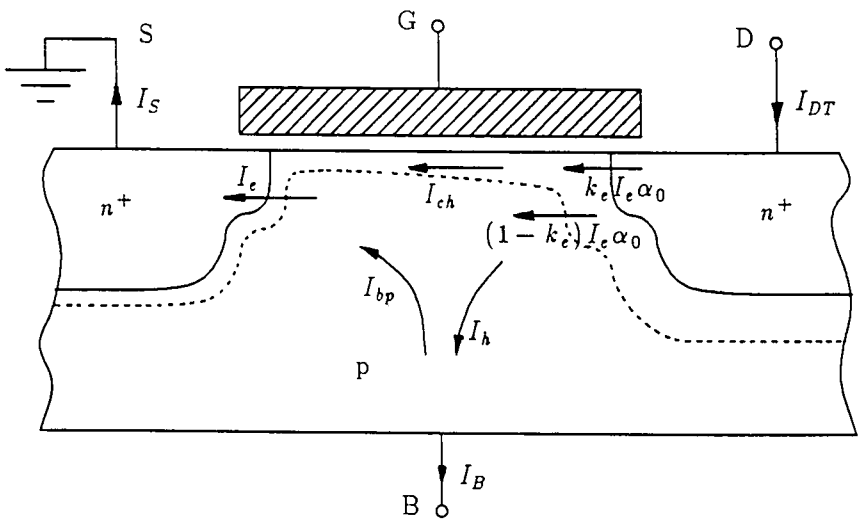

Fig. 2.3. Schematic diagram showing currents in a n-MOS transistor after turn-on of the source-substrate junction

The substrate current is the difference between the hole current I_h and the base current I_{bp} of the parasitic bipolar transistor:

$$I_B = I_h - I_{bp} \tag{2.7}$$

The base current is the difference between the emitter and the collector currents:

$$I_{bp} = I_e - I_c = I_e(1 - \gamma\alpha_T) = I_e(1 - \alpha_0) \tag{2.8}$$

where

γ is the injection efficiency of the source junction

α_T is the base transport factor

$\alpha_0 = \gamma\alpha_T$ is the common base current gain.

The hole current is given by

$$I_h = (M - 1)(I_{ch} + k_e\alpha_0 I_e) \tag{2.9}$$

where k_e is the fraction of the electrons collected by the drain that go through the high-field region causing additional ionization, to the total number of electrons collected by the drain.

The substrate current can now be expressed as

$$I_B = (M - 1)(I_{ch} + k_e\alpha_0 I_e) - I_e(1 - \alpha_0) \tag{2.10}$$

and the total drain current is equal to

$$I_{DT} = I_S + I_B = M(I_{ch} + k_e\alpha_0 I_e) + (1 - k_e)\alpha_0 I_e \tag{2.11}$$

After the source-substrate junction is turned on, the forward-bias voltage V_F remains nearly fixed at about 0.65 V, even though the substrate current rapidly increases. This behavior can be explained by the conductivity modulation of the substrate that occurs when electron injection level is

above the substrate doping concentration. In effect, the substrate resistance is decreased and the voltage drop $I_B R_B$ remains almost constant. Also, an increase in voltage drop across the source series resistance due to higher source current tends to lower the forward bias voltage V_F (eq. 2.1).

To find a condition for source-drain breakdown (providing the source-substrate junction is turned on) lets substitute I_B in (2.1) with (2.10) and solve for I_e to get:

$$I_e = \frac{(M-1)I_{ch}R_B - V_{SB} - I_S R_S - 0.6}{[1 - \alpha_0 - (M-1)k_e\alpha_0]R_B} \tag{2.12}$$

From (2.12) we can see that when the dominator approaches zero, the injection current increases rapidly causing the total drain current to be also very large. Thus, the breakdown condition is expressed by

$$1 - \alpha_0 - (M-1)k_e\alpha_0 = 0 \tag{2.13}$$

or

$$M - 1 = \frac{1 - \alpha_0}{k_e\alpha_0} = \frac{1}{k_e\beta} \tag{2.14}$$

where β is the effective common-emitter current gain of the parasitic bipolar transistor.

In summary, two conditions have to be satisfied before source-drain breakdown can occur:

1. $V_F \approx 0.65\,V$, i.e. the source-substrate junction has to be turned on
2. The avalanche multiplication factor has to be sufficiently large to cause a significant positive feedback effect (eq. 2.14)

For transistors with high substrate doping concentration (small R_B) and/or

low gate voltages (small channel current) the first condition is the governing factor. I-V characteristics for this case are shown in Fig. 2.4.

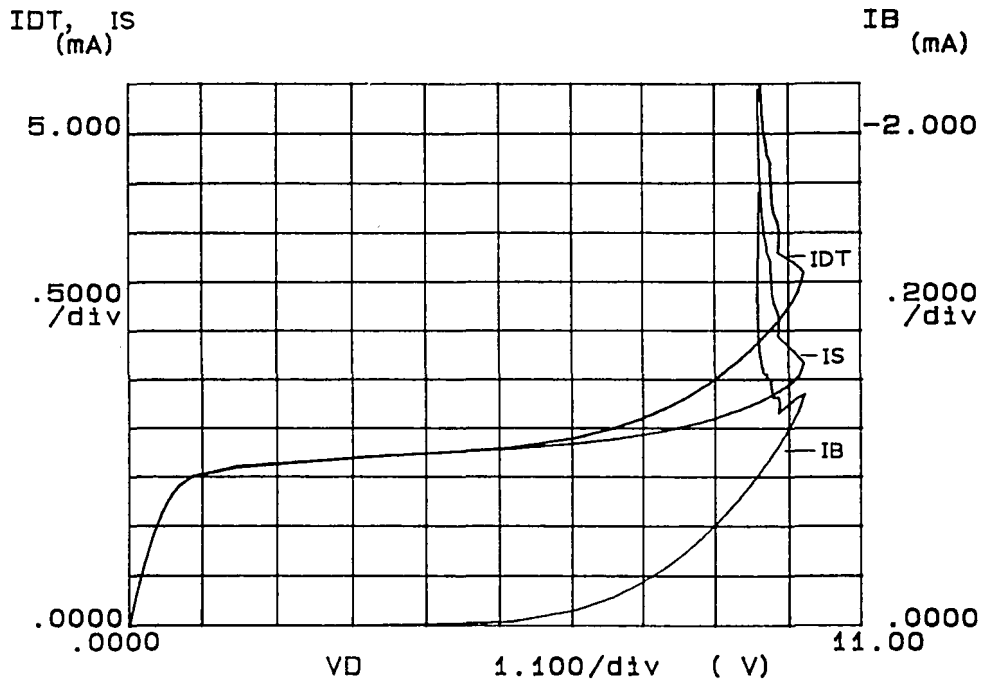

Fig. 2.4. Measured I-V characteristics of a n-MOS LDD transistor;
L_{eff}= 1.0 μm, R_B= 600 Ω, V_G= 2 V

For source-drain voltages below $V_{DS} \approx 5\ V$, which is the normal operating range for MOS transistors, the substrate current is negligible. As V_{DS} is increased above 5 V, the hole current starts to flow raising the substrate potential next to the source and increasing the source current (similar to an external back-gate bias V_{SB}). The total drain current, as a sum of the source and the substrate currents, also increases. When the forward bias voltage V_F reaches about 0.65 V, the source-substrate junction becomes turned on injecting electrons to the substrate which generate more holes by impact ionization. The hole current further increases V_F voltage which results in even higher electron injection. This positive feedback takes place when the

value of the multiplication factor M is already higher than the one expressed by (2.14)[1] , so when the feedback is initiated, the source-drain voltage snaps back to the value that corresponds to M expressed by (2.14). The drain current increases rapidly due to the feedback effect, even though the drain voltage ramains constant or even decreases.

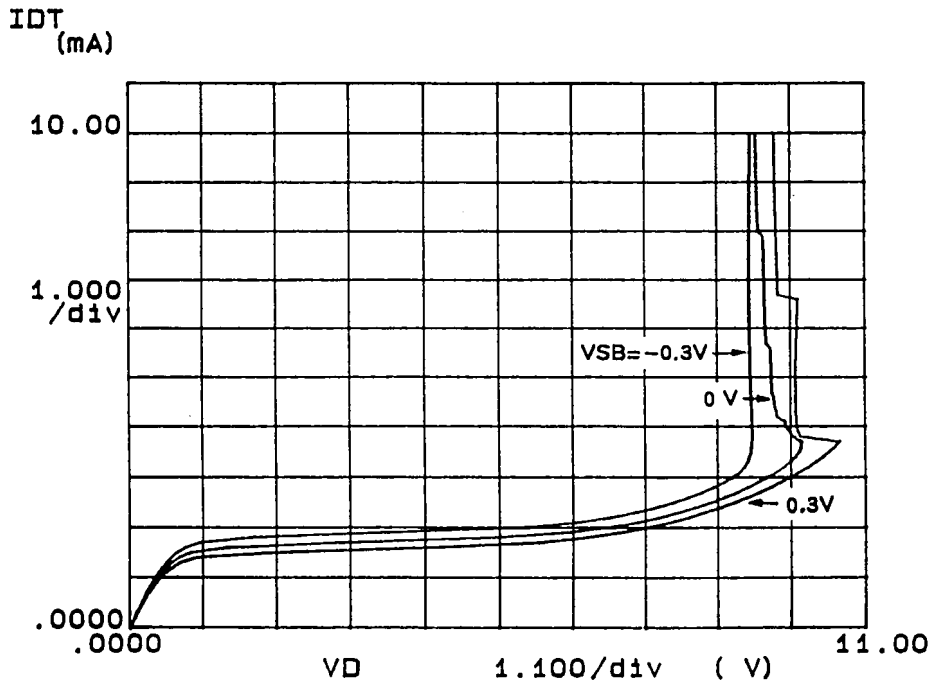

Fig. 2.5. $I_{DT} - V_D$ characteristics with variable back-gate bias; $V_G = 2V$

By applying an external back-gate bias V_{SB} one can change the breakdown voltage (snap-back voltage) or even eliminate the snap-back as seen in Fig. 2.5. A positive V_{SB} (i.e., the source potential is higher than the substrate potential) reverse-biases the source-substrate junction, such that the

1. The condition (2.14) was met at a lower V_{DS} (lower M) than the the breakdown voltage, but the breakdown did not occur because the source-substrate junction had not yet been turned on, i.e. $V_F < 0.65$ V.

condition $V_F \approx 0.65\,V$ will not occur until large enough current flows through the substrate which requires higher V_{DS} (higher M). In effect, the breakdown voltage is increased. Conversly, when V_B is negative but higher than - 0.65 V, the source junction is forward biased (but not yet turned on), so a lower substrate current (lower M) is sufficient to turn it on. Thus, both breakdown conditions are met at lower source-drain voltage and the drain current abruptly increases without the snap-back behavior.

For transistors with lightly doped substrates (large R_B) and/or high gate voltages (larger channel current) the second condition determines the breakdown. I-V characteristics for this case are shown in Fig. 2.6. LDD transistors usually have a high substrate doping concentration to avoid source-to-drain punch-through. Thus, a similar effect to the large R_B can be accomplished by connecting a large external resistance to the substrate terminal.

Fig. 2.6(a) shows $I_{DT} - V_{DS}$ and $I_B - V_{DS}$ characteristics of the LDD MOS transistor with a 22 $k\Omega$ external resistor connected to the substrate. Because the total substrate resistance ($R_B + R_{ext}$) is now much larger, a much lower substrate current (lower V_{DS}) is sufficient to turn on the source-substrate junction. However, there is no appreciable electron injection from the source.[2] This can be explained as follows. In the presence of the large external resistance the substrate current is limited to about 0.65 V/R_{ext} and the excessive holes are injected to the source instead of flowing to the substrate terminal. These holes are traveling a very short distance

2. A small jump in the total drain current ($\approx$ 0.5 mA) at $V_{DS} = 6\,V$ is caused by the self-back-gate biasing voltage $I_B(R_B + R_{ext})$.

from the drain junction to the source. Since the resistance of this section of the substrate is very small, the voltage drop caused by the flow of the hole current is also very small.

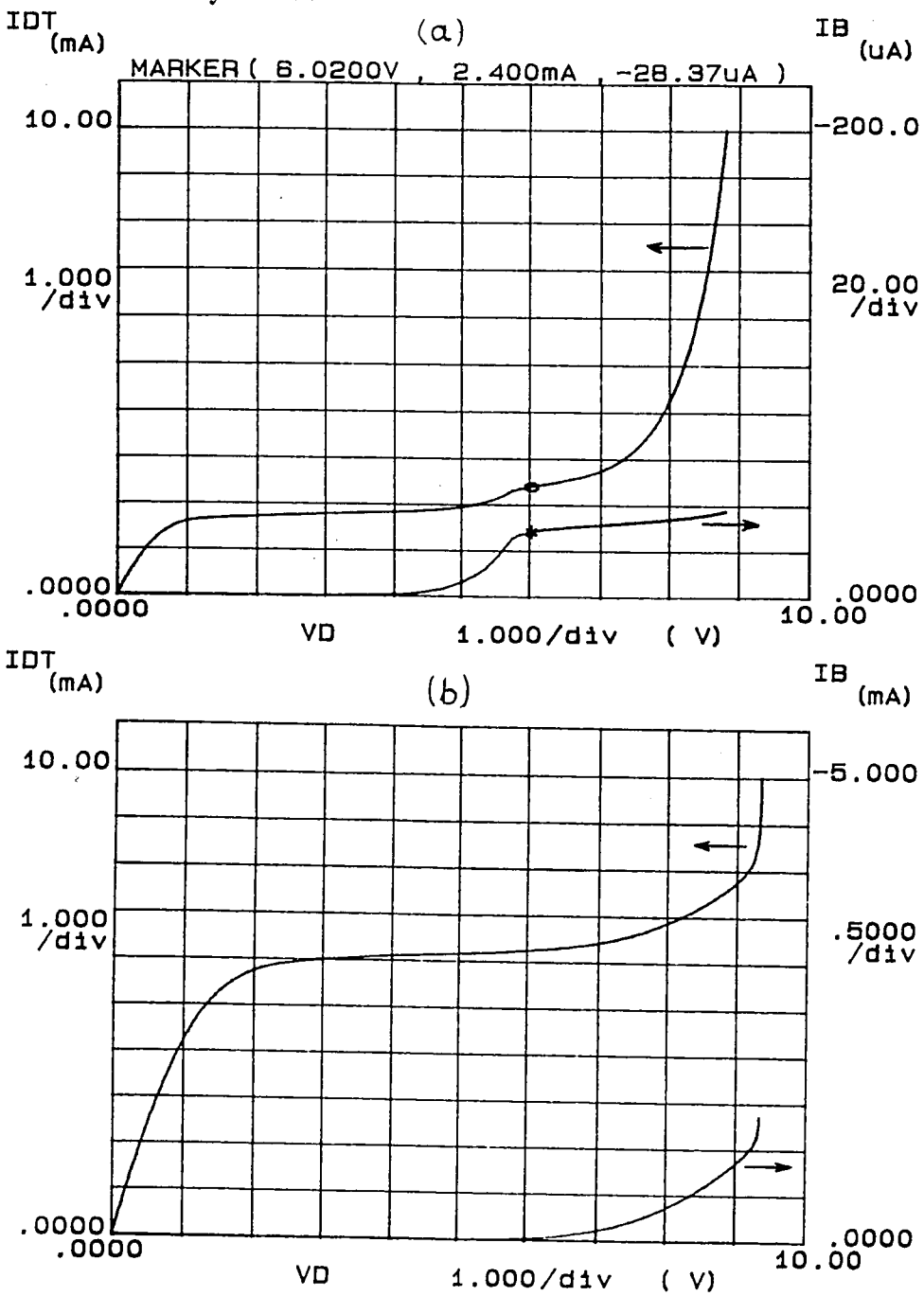

Fig. 2.6. Measured I-V characteristics of a n-MOS LDD transistor: a) $V_G = 2\,V$, $R_{ext} = 22\,k\Omega$, b) $V_G = 4\,V$, $R_{ext} = 0$.

Thus, after the initial fast increase of the forward biasing voltage, an additional increase above 0.65 V is much slower which translates to a gradual increase of the injection and total drain currents. Both currents start to increase rapidly only when the second breakdown condition is met, i.e. the multiplication factor approaches the value expressed by eq. 2.14.

Fig. 2.6(b) shows I-V characteristics for $V_G = 4V$ and $R_{ext} = 0$. In this case the channel current is higher than at $V_G = 2V$, so is the substrate current. Thus, the source junction becomes turned on at lower V_{DS}. Both breakdown conditions are met at about the same V_{DS} and the total drain current increases abruptly without the snap-back behavior.

CHAPTER 3

3. Theoretical I-V characteristics in the breakdown mode

3.1 Calculation of I-V curves

Theoretical $I_{DT} - V_{DS}$ and $I_B - V_{DS}$ curves of a LDD MOS transistor that include the breakdown region are calculated by a computer program written in Microsoft's Quick Basic which can be run on IBM compatible personal computers. The currents are calculated for each source-drain voltage V'_{DS} that is applied to the transistors' terminals.

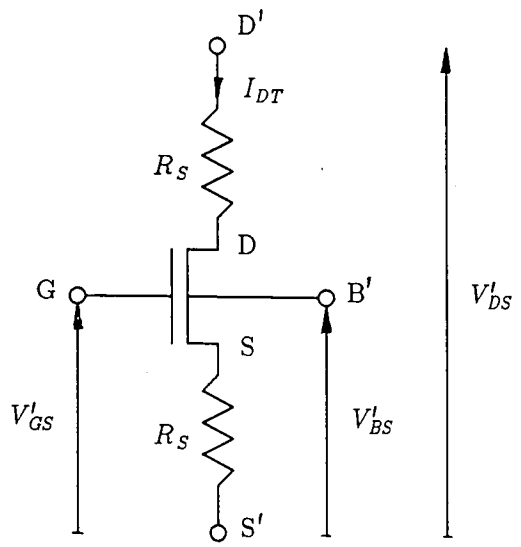

Fig. 3.1. LDD transistor with source and drain series resistances.

Because of the voltage drop across the source and drain series resistances which include the resistance of LDD regions as well as contact and wiring resistances, the "internal" voltages that appear in the expressions for the currents are lower than the voltages applied to the transistors' terminals. The relations between them are (Fig. 3.1):

$$V_{DS} = V'_{DS} - 2I_{DT}R_S \tag{3.1}$$

$$V_{GS} = V'_{GS} - I_{DT}R_S \tag{3.2}$$

$$V_{BS} = V'_{BS} - I_{DT}R_S \tag{3.3}$$

where $V'_{DS}, V'_{GS}, V'_{BS}$ represent the transistor terminals' biases and V_{DS}, V_{GS}, and V_{BS} are the "internal" voltages.

The drain and substrate currents are calculated in three distinct regions as shown in Figure 3.2: the linear region (1), the saturation region (2), and the saturation-breakdown region (3).

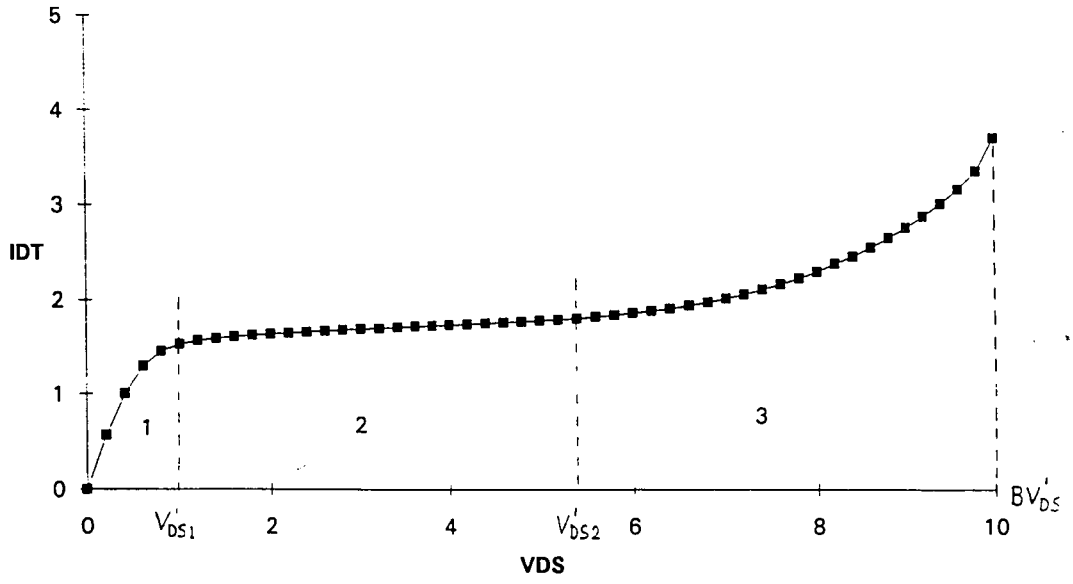

Fig. 3.2 $I_{DT} - V_{DS}$ curve devided into three regions:
linear (1), saturation (2), and saturation-breakdown (3).

Linear Region

This region extends from 0 to V'_{DS1} defined as

$$V'_{DS1} = V_{Dsat} + 2I_{Dsat}R_S \tag{3.4}$$

where V_{Dsat} is the "internal" saturation voltage and I_{Dsat} is the saturation

current. The drain current is calculated using the expression proposed by White et al. [12] and modified here to account for short channel effects by introducing a short channel factor FSC as in [13]

$$I_{DT}(1) = \frac{\mu_0 C_{ox}(W/L)(f - FSC\lambda g)}{1 + (\theta_S/V_{DS})(f + FSC\lambda g) + (V_{DS}/LE_{Cy})} \tag{3.5}$$

where

$$f = (V_{GS} - V_{FB} - 2\phi_F)\, V_{DS} - \frac{1}{2}V_{DS}^2$$

$$g = \frac{2}{3}[(V_{DS} + 2\phi_F + V_{SB})^{\frac{3}{2}} - (2\phi_F + V_{SB})^{\frac{3}{2}}]$$

$$\theta_S = \frac{\epsilon_{ox}}{2\epsilon_{Si}x_{ox}E_{Cx}}$$

θ_S is the surface roughness scattering parameter,

$$\lambda = \frac{\sqrt{2\epsilon_{Si}qN_A}}{C_{ox}}$$

is the body-effect parameter, E_{Cy} is the parallel critical electric field, E_{Cx} is the normal critical electric field.

The short channel factor FSC is expressed as

$$FSC = 1 - \frac{FXS + FXD}{2} \tag{3.6}$$

where

$$FXS = \left(\frac{x_j}{L}\right)\left(\left(1 + 2\frac{x_s}{x_j}\right)^{\frac{1}{2}} - 1\right)$$

$$FXD = \left(\frac{x_j}{L}\right)\left(\left(1 + 2\frac{x_d}{x_j}\right)^{\frac{1}{2}} - 1\right)$$

$$x_s = \frac{2\epsilon_{Si}}{qN_A}(2\phi_F + V_{SB})^{\frac{1}{2}}$$

$$x_d = \frac{2\epsilon_{Si}}{qN_A}(2\phi_F + V_{DS} + V_{SB})^{\frac{1}{2}}$$

For each V_{DS}, the value of I_{DT} is found by solving numerically the equation

$$I_{DT} - f(I_{DT}) = 0$$

where $f(I_{DT})$ is the RHS of (3.5).

Saturation Region

This region extends from V'_{DS1} defined previously, to V'_{DS2} defined as a source-drain voltage at which V_F is very small (e.g. 0.005 V), such that the injection current I_e is negligible. The total drain and substrate currents in this region are given by

$$I_{DT} = M\, I_{ch} \tag{3.7}$$

$$I_B = (M - 1)\, I_{ch} \tag{3.8}$$

where I_{ch} is the channel current expressed as

$$I_{ch} = \frac{I_{Dsat}}{1 - L_{sat}/L} \tag{3.9}$$

where L_{sat} is the length of the saturation region. The substrate current is negligible (M $\approx$ 1) up to $V_{DS} \approx 5\,V$, and the total drain current is equal to the channel current.

Saturation-Breakdown Region

This region extends from V'_{DS2} to BV'_{DS} - the breakdown voltage. In this range of V_{DS} an appreciable generation of hole-electron pairs takes place, and the flow of the substrate current has a noticeable impact on the

transistor characteristics. No attempt has been made to calculate the theoretical characteristics in the negative resistance region i.e. after V_{DS} snaps back, because of the complex nature of the positive feedback.

Equations (2.10) and (2.11) are used for calculating the substrate and the total drain current, respectively. The self back-gate biasing by the substrate current is accounted for by replacing the external back-gate biase V_{SB} with $V_{SB} - I_B R_B$ in all equations that are used in calculations. The injection current I_e is found by solving numerically the equation:

$$I_e - f(I_e) = 0$$

where $f(I_e)$ is the RHS of (2.5) with V_F, I_B, and I_S given by (2.1), (2.10), and (2.6), respectively.

The common-base current gain α_0 is estimated from the second condition for the breakdown (2.14), together with (2.4) by measuring the source and substrate currents just before the breakdown occurs,

$$M - 1 = \frac{1}{k_e \beta} \approx \frac{I_B}{I_S} \tag{3.10}$$

The ratio of these two currents for $V_{GS} = 4\,V$ is found to be 0.15 giving the value of $k_e\beta \approx 6.7$. Assuming $k_e = 0.75$[1] , the estimated value of α_0 is 0.9. Even though this is a pretty rough estimation, the impact of this inaccuracy on the shape of theoretical I-V curves is small because the injection current is very small until the source junction becomes fully turned on, which occurs only when V_{DS} approaches the breakdown value.

1. Most of the electrons injected out of the source are pushed towards the channel [11], and go through the high field region.

3.2 Calculation of Avalanche Multiplication Factor

Assuming equal ionization rates for holes and electrons, the multiplication factor can be expressed as

$$M = \frac{1}{1 - \int_{-L_{sat}}^{y_d} \alpha(E_y)\, dy} \tag{3.11}$$

where $\alpha(E_y)$ is the ionization rate given by (1.6), $y = -L_{sat}$ is the location of the pinch-off point, and y_d is the edge of the depleted region as shown in Figure 3.3. Thus, in order to calculate M, the profile of the electric field along the channel $E_y(y)$, as well as L_{sat} and y_d have to be known. These parameters are found from the electric field model for LDD structures [10], which is slightly modified here to account for short-channel effects and source/drain series resistances. The outline of this model is presented below.

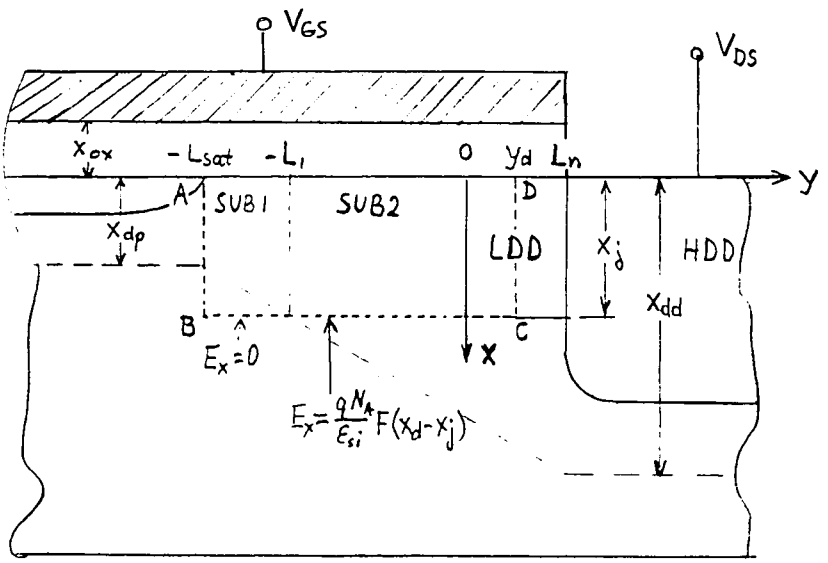

Fig. 3.3. Cross section of a LDD MOS transistor near the drain.

Applying Gauss' law to the rectangle ABCD (Fig. 3.3) and differentiating the obtained equation with respect tc the lateral dimension y, we get the

differential equation

$$\frac{\partial E_y(x,y)}{\partial y} = \frac{q}{\epsilon_{Si} x_j}\left(\frac{Q_m}{q} + N x_j\right) - \frac{E_x(0,y) - E_x(x_j,y)}{x_j} \tag{3.12}$$

where N is the doping density of the particular region, SUB1, SUB2, LDD, or HDD where y resides, Q_m is the mobile charge density per unit area, which is given by

$$Q_m = C_{ox}(V_{GS} - V_{TH} - V_{Dsat}) \tag{3.13}$$

V_{TH} is the threshold voltage expressed as

$$V_{TH} = V_{FB} + 2\phi_F + FSC\,\frac{qN_A x_{dp}}{C_{ox}} \tag{3.14}$$

where FSC is the short-channel factor given by (3.6), and x_{dp} is the depletion width in the substrate at the pinch-off point. Defining the effective gate voltage as $V_{GSeff} = V_{GS} - V_{FB} - 2\phi_F$ and substituting (3.14) into (3.13), Q_m can be expressed as

$$Q_m = C_{ox}(V_{GSeff} - V_{Dsat}) - qN_A x_{dp} FSC \tag{3.15}$$

If we neglect trapped charge at the oxide-silicon interface, then the normal electric field at the interface is given by

$$E_x(0,y) = \frac{C_{ox}}{\epsilon_{Si}}[V_{GSeff} - V(y)] \tag{3.16}$$

The normal electric field at the junction depth is zero in the SUB1 region, defined as a section of the saturation region where $x_d(y) < x_j$.

In the SUB2 region, defined as a section of the saturation region where $x_d(y) > x_j$, the normal electric field is given by

$$E_x(x_j, y) = \frac{qN_A}{\epsilon_{Si}} F\left[x_d(y) - x_j\right] \tag{3.17}$$

where F is the fraction of depletion charge below x_j at y which contributes to the normal field at the junction depth, and $x_d(y)$ is the depletion layer boundary, which can be expressed (assuming linear variation with y) as

$$x_d(y) = k(y + L_{sat}) + x_{dp}$$

$$k = \frac{x_{dd} - x_{dp}}{L_{sat} + L_n}$$

where x_{dd} is the edge of the depletion region under the HDD region and L_n is the length of the LDD region.

In the LDD region the normal electric field at the junction depth is constant, and equal to

$$E_x(x_j, y) = \frac{qN_A}{\epsilon_{Si}} F\left(kL_{sat} + x_{dp} - x_j\right) \tag{3.18}$$

and finally, in the HDD region $E_x(x_j, y) = 0$.

Differential equation (3.12) is solved with the following boundary conditions

1. At the pinch-off point, $y = -L_{sat}$

   $$V = V_{Dsat}, \quad E_y = E_{sat}$$

2. The channel potential and the electric field are continuous between the regions: SUB1, SUB2, LDD, and HDD.
3. At the end of the depletion edge, $y = y_d$, and

   a. If y_d lies within HDD region (the LDD region is fully depleted)

   $$V = V_{DS}' - I_{DT}(2R_S - R_{LDD}), \quad E_y = 0$$

b. If y_d lies within the LDD region (the LDD region is partially depleted)

$$V = V'_{DS} - I_{DT}\,[2R_S - (R_{LDD} - R_D)]$$

$$E_y = \frac{R_D I_{DT}}{L_n - y_d}$$

where $R_S = R_C + R_{LDD}$ is the total series resistance of the drain (or source) that includes the contact and wiring resistance R_C, and the resistance of the LDD region R_{LDD}, R_D is the resistance of the undepleted section of the LDD region (Fig 3.4), and can be written as

$$R_D = \frac{\rho(L_n - y_d)}{W x_j}$$

where ρ is the resistivity of the LDD region and W is the channel width.

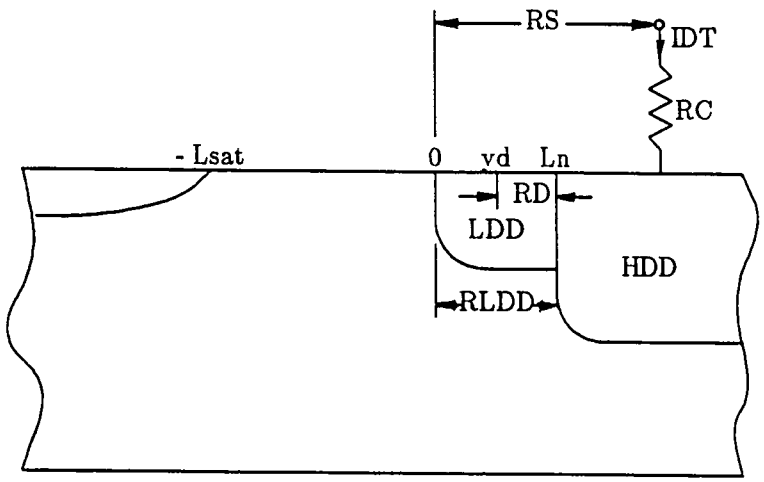

Fig. 3.4. Diagram showing a total series resistance of the drain.

The solution of (3.12) for the channel potential, in the case where there are two SUB regions, is

$$V_1(y) = V_{Dsat} + \phi_A \cosh\left(\frac{y + L_{sat}}{l}\right) + l\,E_{sat}\sinh\left(\frac{y + L_{sat}}{l}\right) - \phi_A, \quad \text{in SUB1}$$

$$V_2(y) = V_1(y) + \phi_M \left[\sinh\left(\frac{y + L_1}{l}\right) - \left(\frac{y + L_1}{l}\right) \right], \qquad \text{in SUB2}$$

$$V_3(y) = V_2(y) - \phi_M \left[\sinh\left(\frac{y}{l}\right) - \left(\frac{y}{l}\right) \right] - \phi_D \left[\cosh\left(\frac{y}{l}\right) - 1 \right], \qquad \text{in LDD}$$

$$V_4(y) = V_3(y) - (\phi_{DD} - \phi_D) \left[\cosh\left(\frac{y - L_n}{l}\right) - 1 \right], \qquad \text{in HDD}$$

and the solution for the lateral electric field is

$$E_{y1}(y) = \frac{\phi_A}{l} \sinh\left(\frac{y + L_{sat}}{l}\right) + E_{sat} \cosh\left(\frac{y + L_{sat}}{l}\right), \qquad \text{in SUB1}$$

$$E_{y2}(y) = E_{y1}(y) + \frac{\phi_M}{l} \left[\cosh\left(\frac{y + L_1}{l}\right) - 1 \right], \qquad \text{in SUB2}$$

$$E_{y3}(y) = E_{y2}(y) - \frac{\phi_M}{l} \left[\cosh\left(\frac{y}{l}\right) - 1 \right] - \frac{\phi_D}{l} \sinh\left(\frac{y}{l}\right), \qquad \text{in LDD}$$

$$E_{y4}(y) = E_{y3}(y) - \frac{(\phi_{DD} - \phi_D)}{l} \sinh\left(\frac{y - L_n}{l}\right), \qquad \text{in HDD}$$

where

$$\phi_A = \phi_0 \left[1 - \frac{x_{dp}}{x_j} FSC \right]$$

$$\phi_0 = \frac{qN_A x_j}{C_{ox}}, \qquad \phi_M = \phi_0 Fk \frac{l}{x_j}$$

$$\phi_D = \phi_0 \left[1 - \frac{N_D}{N_A} \right], \quad \phi_{DD} = \phi_0 \left[1 - \frac{N_{DD}}{N_A} \right]$$

$$l = \sqrt{\frac{\epsilon_{Si} x_j}{C_{ox}}}, \qquad L_1 = L_{sat} + \frac{x_{dp} - x_j}{k}$$

The program, whose flowchart is shown in Figure 3.5, calculates theoretical $I_{DT} - V_{DS}$ and $I_B - V_{DS}$ curves of a LDD MOS transistor. A part of the program that calculates the saturation parameters and the lateral electric field is based on the program MIKIMOS [10].

After starting the program, the user is asked to enter the gate and the substrate biases, the increment at which the source-drain voltage is swept, and the channel length. First, the program calculates the "internal" saturation voltage, the saturation current, and the "real" saturation voltage between the source and drain terminals V'_{DS1}. Then, the source-drain voltage is swept from 0 to the value at which both breakdown conditions are met. This is the breakdown voltage. Depending on the range of V_{DS}, the drain and substrate currents are calculated in three regions: linear, saturation, and saturation-breakdown. The calculated values of the drain and substrate currents are written to a data file. A typical output of the program is shown in Figure 3.6.

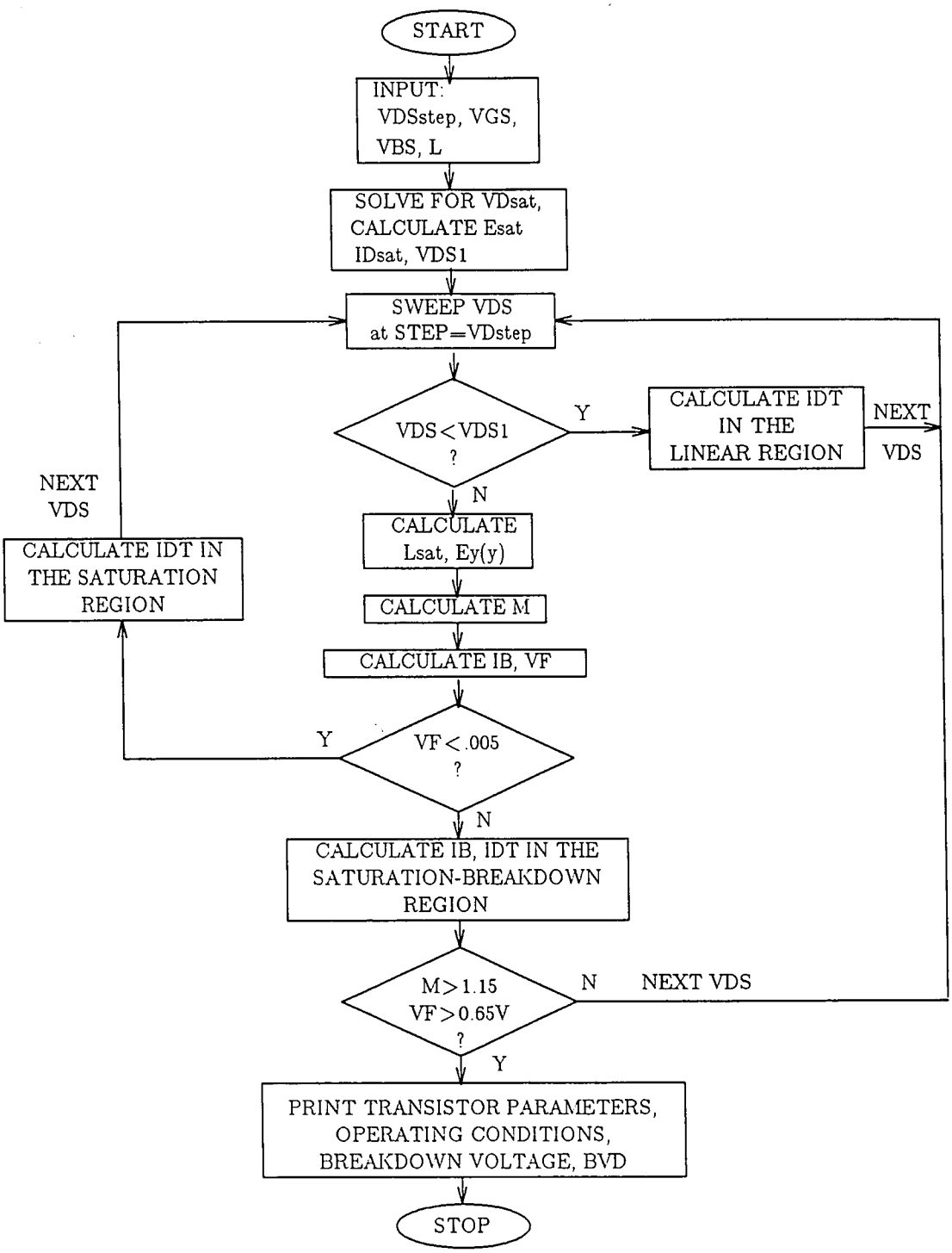

Fig. 3.5. FLOWCHART OF THE QUICK BASIC PROGRAM

```
TRANSISTOR PARAMETERS AND OPERATING CONDITIONS:

VDSstep          [V]              .2
VGS              [V]              2
VBS              [V]              0
L0               [um]             1
NA               [cm^-3]          5.1E+16
ND               [cm^-3]          3E+17
NDD              [cm^-3]          1E+21
Xj               [um]             .25
Xjd              [um]             .44
Ln               [um]             .13
F (fringing factor)               .7
n (saturation level)              .5
VFB              [V]             -.96
EcritL           [MV/cm]          .03
EcritN           [MV/cm]          .8
U0               [cm^2/V-s]       560
UD               [cm^2/V-s]       1000
COX              [F/cm^2]         1.606109E-07
LAMBDA           [V^.5]           .8170148
ALPHA            [cm/V^.5]        1.605909E-05
PHIF             [V]              .3896487
PHIS0            [V]              .7792974
BETA0            [A/V^2]          2.698262E-03
VTH              [V]              .4574412
THETAS           [1/V]            9.527068E-02
RHO              [ohm-cm]         2.080487E-02
RB               [ohm]            600
RS               [ohm]            10
I0               [A]              1E-15

SIMULATION PARAMETERS:

dV (convg)       [V]              .000001
dL (convg)       [cm]             1E-10
dI (convg)       [A]              1E-08
Max # of iterations
for VDsat, Lsat, Yd, IE           100
Max total iter. for Lsat          20

CALCULATION RESULTS:

VDsat            [V]              .9263732
IDsat            [mA]             1.502596
Esat             [MV/cm]          3.628075E-02
BVDbreak         [V]             10.0
```

Fig. 3.6. A typical output of the Quick Basic Program

CHAPTER 4

4. Measurements

4.1 Measuring Technique and Equipment

I-V characteristics of the LDD MOS transistor were measured with a Hewlett-Packard Model 4145A semiconductor parameter analyzer. The R & K 777 manual prober with Bausch and Lomb microscope was used to make contacts to the bond pads of the measured transistor. A picture of the transistor layout showing the bond pads is presented in Figure 4.1.

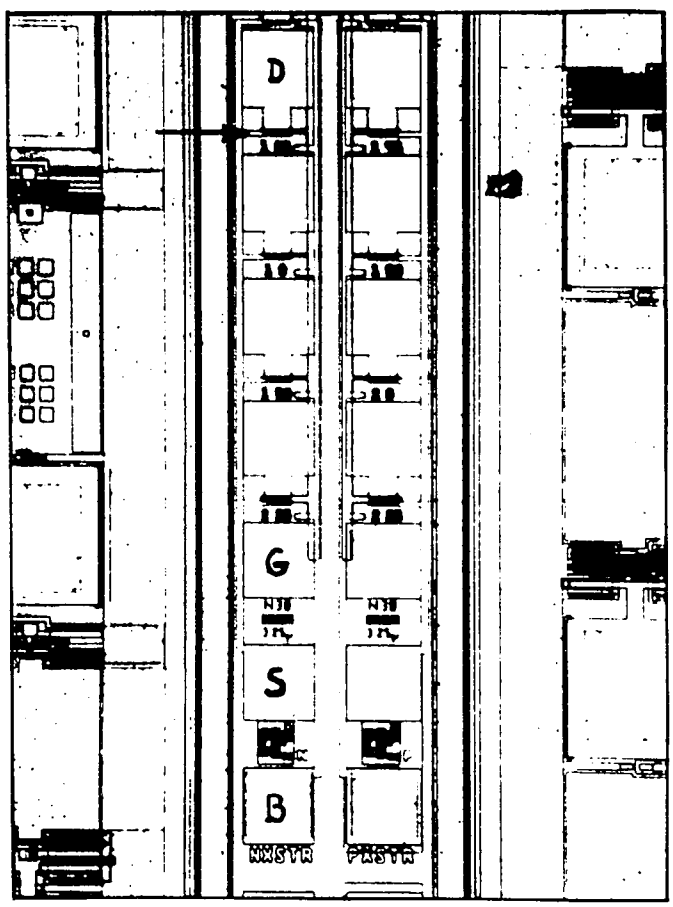

Fig. 4.1. Grid tester with the measured device indicated by an arrow.

The devices investigated in this thesis were fabricated with 1.25 μm CMOS single level metal technology. The measured transistor (indicated by an arrow in Fig. 4.1) is a part of the standard grid tester. Its nominal (coded) channel length is 1.25 μm, the electrical channel length is 1.0 μm, and the channel width is 30 μm.

In order to measure I-V characteristics in the snap-back region, the SMU (Stimulus/Measurement Unit) channel that is connected to the drain of the device should be in the current source/voltage monitor mode. In this mode, the drain current is swept from 0 to a predetermined maximum in small increments e.g. 0.1 mA, and the corresponding source-drain voltage is measured. Otherwise, i.e. when the SMU channel is in the voltage source/current monitor mode, as soon as V_{DS} reaches the breakdown value the drain current will rapidly increase without the snap-back and unless the current is limited to several miliamps, a distructive breakdown will occur.

CHAPTER 5

5. Conclusions and Recommendations

5.1 Comparison Between Model and Experiments

Figure 5.1 shows predicted by the model I-V characteristics as compared with the measured ones for $V_{GS}=2\,V$. There is a good agreement between these curves. The biggest deviation of the calculated drain current from the measured one is found at the breakdown voltage and is equal to 13%. In the saturation region the deviation is less than 7%.

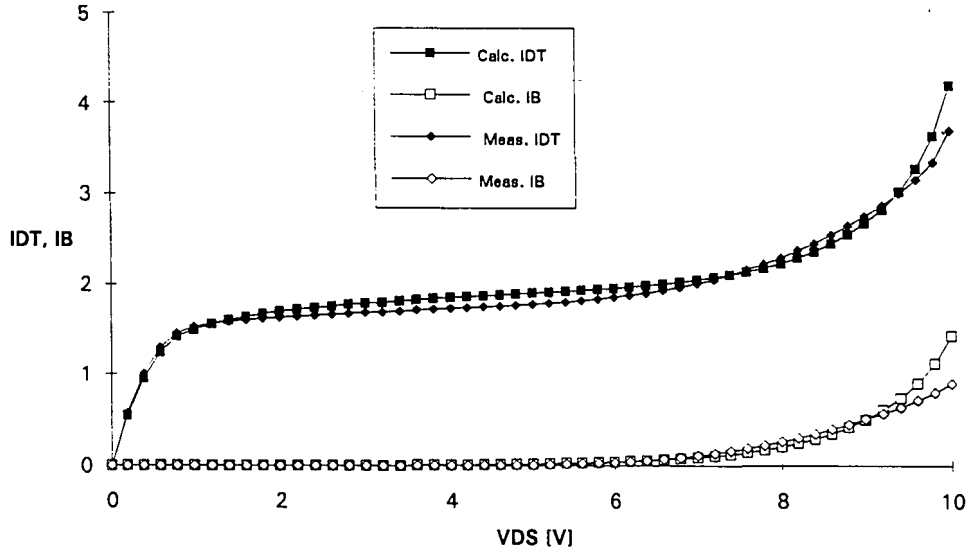

Fig. 5.1. Calculated and measured drain and substrate currents for $V_{GS}=2\,V,\ V_{SB}=0$

The drain and substrate currents for $V_{GS}=4\,V$ are shown in Figures 5.2 and 5.3 respectively. The maximum deviation of the calculated drain current from the measured is found in the saturation region and is about 13%. The explanation for this is that the saturation region length Lsat predicted by

the model is too high, causing the calculated channel current to be also higher than the measured one (eq. 3.9). There is a very good agreement between the measured and calculated substrate currents.

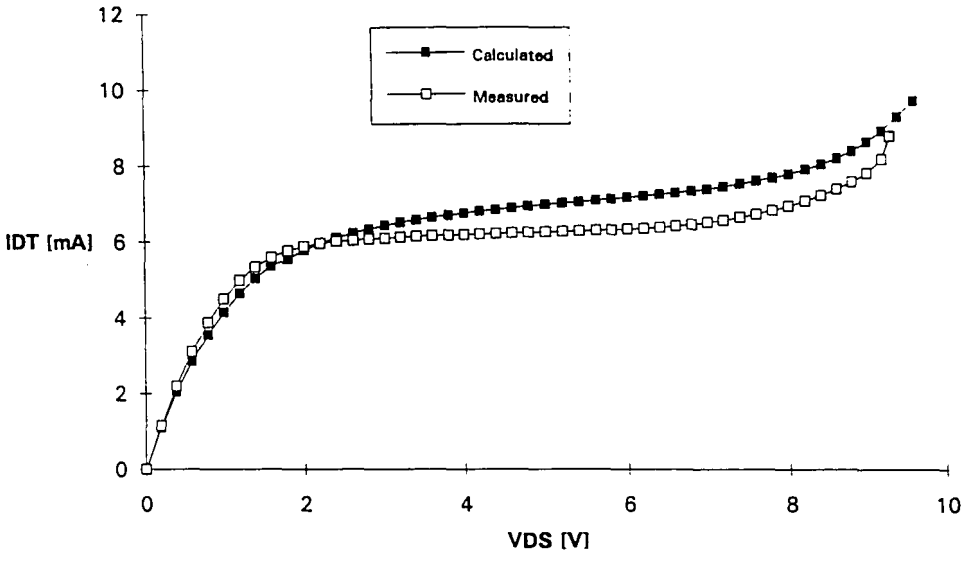

Fig. 5.2. Calculated and measured drain currents for $V_{GS} = 4\,V$

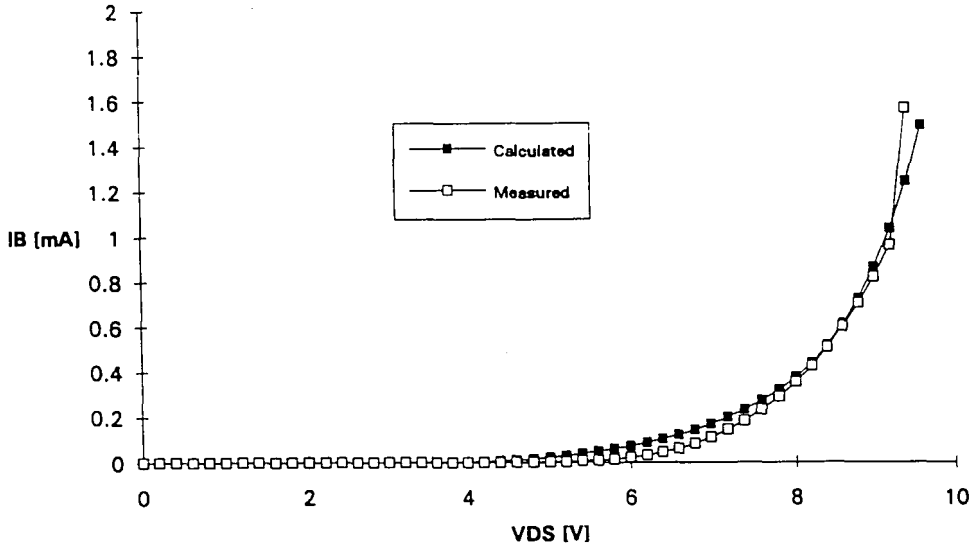

Fig. 5.3. Calculated and measured substrate currents for $V_{GS} = 4\,V$

Figure 5.4 shows calculated and measured drain currents for the gate bias $V_{GS} = 2\,V$ and the substrate biases $V_{SB} = -0.5\,V$ and $V_{SB} = 0.5\,V$. There is a very good agreement between the curves except for the source-drain voltages close to breakdown.

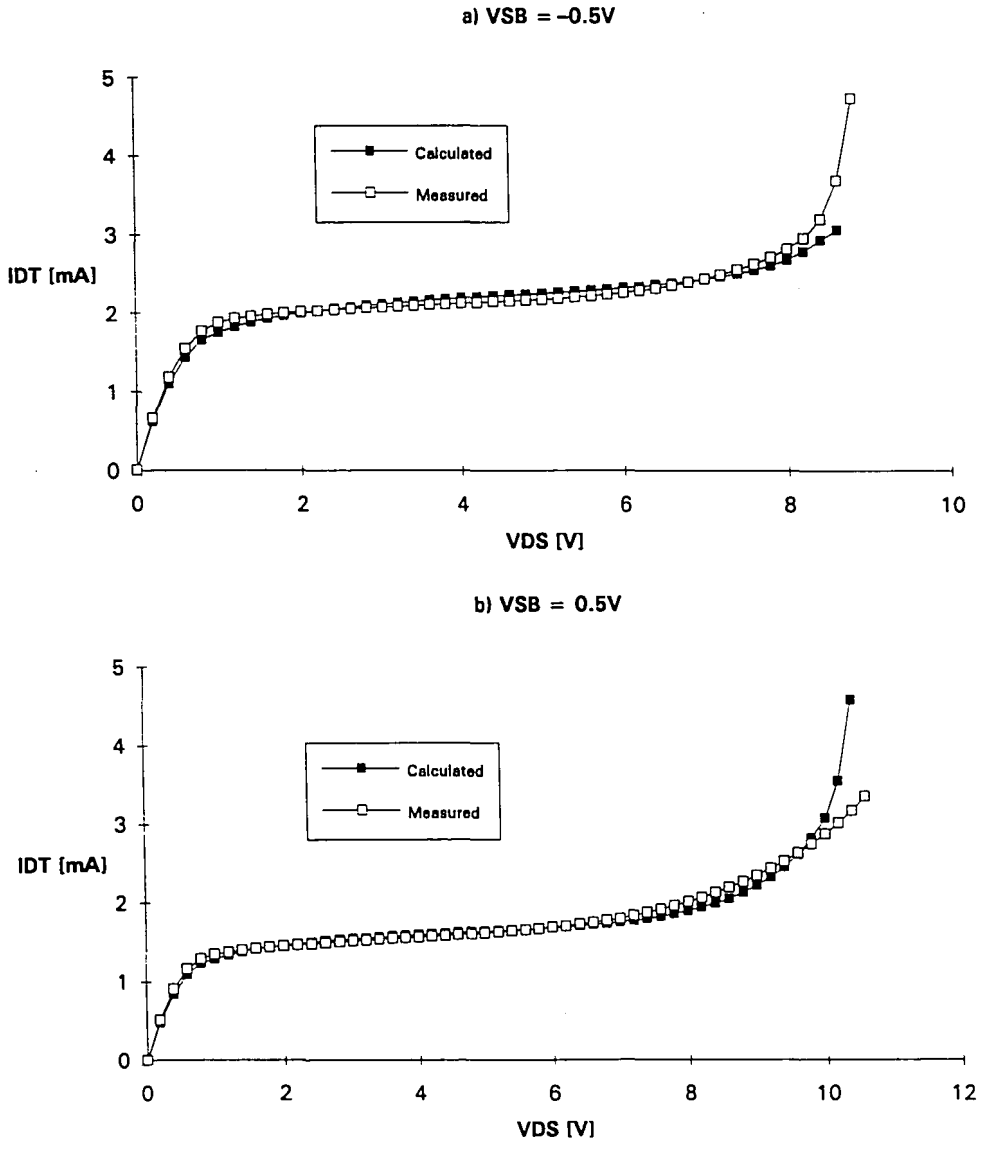

Fig. 5.4. Calculated and measured drain currents for $V_{GS} = 2\,V$ and $V_{SB} = -0.5\,V$ and $V_{SB} = 0.5\,V$.

5.2 Recommendations

In this thesis only one type of LDD MOS transistor was investigated to verify the breakdown model, i.e. the n-channel device with 1.0 μm electrical channel length. Further study should be pursued to determine the validity of the model for MOS transistors with different channel lengths, substrate doping concentrations (substrate resistance), and the dimensions and doping concentrations of the LDD region (lateral electric field near the drain).

```
'                    APPENDIX A
'
'                Quick Basic Program
'=============================================================================
      'This program calculates IDT vs VDS characteristic of a LDD MOS
      'transistor including the breakdown region.
      'ZBIGNIEW KOZLOWSKI, LEHIGH UNIVERSITY. APRIL 10, 1992.
'=============================================================================
      DECLARE FUNCTION PHIS! (IB!)
      DECLARE FUNCTION FSC! (X!)
      DECLARE SUB FindIDlin (X!)
      DECLARE FUNCTION FofID! (X!)
      DECLARE SUB CalcPars ()
      DECLARE SUB GetVF ()
      DECLARE SUB GetIDT3 ()
      DECLARE SUB FindIE (X!, I%)
      DECLARE FUNCTION FofIE! (X!)
      DECLARE SUB GetMfactor ()
      DECLARE FUNCTION GofYd! (YdP!)
      DECLARE FUNCTION EofY! (Y!, LsatP!)
      DECLARE FUNCTION SINH! (X!)
      DECLARE FUNCTION COSH! (X!)
      DECLARE SUB GetVEYd (YdP!, LsatP!, VYd!, EYd!)
      DECLARE FUNCTION FofLsat! (LsatP!)
      DECLARE FUNCTION VofY! (Y!, LsatP!)
      DECLARE SUB FindLsat (X!, I%)
      DECLARE SUB FindYd (X!, I%)
      DECLARE SUB GetLsat ()
      DECLARE SUB FindVDsat (X!, I%)
      DECLARE FUNCTION IDsat1! (X!)
      DECLARE FUNCTION IDsat2! (X!)
      DECLARE FUNCTION FofVDsat! (X!)
      DECLARE SUB GetEsat ()
      DECLARE SUB WritePars ()

      DIM SHARED VDS, VD, VGS, VG, VBS, VB, VDSstep
      DIM SHARED L0, W, TOX, U0, NA, ND, NDD, Xj, Xjd, LN, F, NN, VFB
      DIM SHARED ECRITL, ECRITN, UD, VDsat, Esat, IDsat, Emax, Lsat, Yd
      DIM SHARED COX, LAMBDA, ALPHA, PHIF, PHIS0, BETA0, THETAS, VTH, RHO
      DIM SHARED IDT, IB, ICH, IH, IE, I0, M, ke, ALPHA0, RB, RS, VF
      DIM SHARED DVconvg, DLconvg, DIconvg
      DIM SHARED ITERmax%, ITERmaxTot%, ITERtot%

      CLS
      INPUT "Enter VDSstep"; VDSstep    'step of the drain-source voltage
      INPUT "Enter VGS"; VGS            'gate-source voltage
      INPUT "Enter VBS"; VBS            'bulk pot. referenced to the source
      INPUT "Enter L0 in microns"; L0

      'fundamental constants:
      'e0     =permittivity in vacuum (F/cm)
      'qe     =electron charge (C)
      'me     =electron rest mass (kg)
      'kb     =Boltzmann constant (J/C)
      'eox    =permittivity of SiO2 (F/cm)
      'esi    =permittivity of Si (F/cm)
      'vt     =thermal voltage (kT/qe) @300K
      'ni     =intrinsic carrier concentration in Si (cm^-3) @300K
      'vsat   =saturation velocity in Si (cm/s) @300K
      'Ai,Bi  =ionization parameters
```

```
CONST e0 = 8.854188E-14, qe = 1.602189E-19, me = 9.109534E-31
CONST kb = 1.380662E-23, eox = e0 * 3.9, esi = e0 * 11.9, vt = .025852
CONST ni = 1.45131E+10, vsat = 1.035E+07
CONST Ai = 2000000!, Bi = 1750000!

'Transistor parameters and operating conditions:
L0 = L0 * .0001          '[cm]     effective channel length (HDD to HDD)
W = .003                 '[cm]     channel width
TOX = 2.15E-06           '[cm]     gate oxide thickness
U0 = 560!                '[cm^2/Vsec] low field mobility
NA = 5.1E+16             '[cm^-3] substrate doping density
ND = 3E+17               '[cm^-3] LDD doping density
NDD = 1E+21              '[cm^-3] HDD doping density
Xj = .000025             '[cm]     LDD junction depth
Xjd = .000044            '[cm]     HDD junction depth
LN = .000013             '[cm]     LDD region length
F = .7                   '          charge-sharing factor
NN = .5                  '          saturation level parameter
VFB = -.96               '[V]      flatband voltage
ECRITL = 30000!          '[V/cm]   critical field (parallel)
ECRITN = 800000!         '[V/cm]   critical field (normal)
UD = 1000!               '[cm^2/Vsec] mobility of LDD region
I0 = 1E-15               '[A] reverse sat. current of the source junction
ke = .75                 '          fraction of collected electrons that go
                         '          through the drain (high field) region
ALPHA0 = .9              '          common base current gain
RB = 600                 '[OHM]    substrate spreading resistance
RS = 10                  '[OHM]    source, drain series resistance
VDSstop = 12             '[V]      max sweep voltage

'Simulation parameters:
DVconvg = .000001          '[V]  small voltage for convergance
DLconvg = 1E-10            '[cm] small length for convergance
DIconvg = 1E-08            '[A]  small current for convergance
ITERmax% = 100             'max # of iterations for VDsat,Lsat,Yd,IE
ITERmaxTot% = 20           'max total iterations for Lsat & Yd

VG = VGS
VB = VBS
CALL CalcPars              'Calculate additional parameters
CALL GetEsat               'Calculate VDsat,Esat,IDsat

VRS = RS * IDsat           'Voltage drop across the source/drain res.
VDsatReal = VDsat + 2 * VRS  '"Real world" source-drain voltage

PRINT "VDsat [V]      ="; VDsat
PRINT "VDsatReal [V]  ="; VDsatReal
PRINT "IDsat [mA]     ="; IDsat * 1000!
PRINT "Esat  [MV/cm]  ="; Esat * .000001
VDsaturation = VDsatReal
Esaturation = Esat * .000001
IDsaturation = IDsat * 1000!

PRINT "VDS      IDT      IB"

OPEN "C:\IVDATA\IDTx.DAT" FOR OUTPUT AS #1

FOR VDS = 0 TO VDSstop STEP VDSstep
 M = 1
 IF VDS < VDsatReal THEN
```

```
 CALL FindIDlin(IDT)          'Calculate IDT in the linear region (1)
ELSE
 VD = VDS - 2 * VRS           'VD  "internal" source-drain voltage
 VG = VGS - VRS               'VG  "internal" source-gate voltage
 VB = VBS - VRS
 CALL GetLsat                 'Calculate Lsat
 CALL GetMfactor              'Calculate Emax, M
 CALL GetVF                   'Calculate forward bias
 IF VF < .005 THEN
  IDT = M * ICH               'Calculate IDT in the saturation
 ELSE                         'region (2); M ~ 1
  CALL GetIDT3                'Calculate IDT in the saturation-breakdown
                              'region (3); M > 1
 END IF
END IF

PRINT #1, USING "##.##"; VDS; SPC(3);
PRINT #1, USING "##.###"; IDT * 1000!; SPC(3);
PRINT #1, USING "#.###"; IB * 1000!
PRINT USING "##.##"; VDS; SPC(3);
PRINT USING "##.###"; IDT * 1000!; SPC(3);
PRINT USING "#.###"; IB * 1000!

IF VF >= .65 AND M >= 1.15 THEN EXIT FOR
NEXT VDS

CLOSE #1
CALL WritePars

LPRINT ""
LPRINT "     CALCULATION RESULTS:"
LPRINT ""
LPRINT "     VDsat        [V]          "; VDsaturation
LPRINT "     IDsat        [mA]         "; IDsaturation
LPRINT "     Esat         [MV/cm]      "; Esaturation
LPRINT "     BVDbreak     [V]          "; USING "##.#"; VDS
END
```

```
'=============================================================================
     SUB CalcPars
'=============================================================================
     'Additional parameters:
     COX = eox / TOX                          '[F/cm^2]   oxide capacitance
     LAMBDA = SQR(2 * esi * qe * NA) / COX    '[V^.5]     body effect param.
     ALPHA = SQR(2 * esi / (qe * NA))         '[cm/V^.5] dep. widening factor
     PHIF = vt * LOG(NA / ni)                 '[V]        bulk fermi potential
     PHIS0 = 2 * PHIF - VB                    '[V]        surf. pot. at source

     BETA0 = U0 * COX * W / L0                '[A/V^2]    transconductance par.
     VTH = VFB + 2 * PHIF + LAMBDA * FSC(VD) * SQR(PHIS0) '[V] th. voltage
```

```
      THETAS = COX / (2 * esi * ECRITN)        '[1/V]     scattering parameter
      RHO = 1 / (qe * UD * ND)                 '[OHM-CM]  res. of LDD region
      END SUB

'=============================================================================
      FUNCTION COSH (X)
'=============================================================================
      E = EXP(X)
      COSH = (E + 1 / E) / 2
      END FUNCTION

'=============================================================================
      FUNCTION EofY (Y, LsatP)
'=============================================================================
      Xdp = ALPHA * SQR(PHIS(IB) + VDsat)      'Dep. region edge at the
                                               'pinch-off point
      Xdd = ALPHA * SQR(PHIS(IB) + VD) + Xjd   'Dep. region edge at HDD
      l = SQR(Xj * esi / COX)                  '[cm] characteristic length
      k = (Xdd - Xdp) / (LsatP + LN)           '~Slope of depletion width edge
      L1 = LsatP + (Xdp - Xj) / k              '~[cm] Y @ dep. width=Xj
      P0 = qe * NA * Xj / COX                  ' [V]
      PA = P0 * (1 - (Xdp / Xj) * FSC(VD))     ' [V]
      PD = P0 * (1 + ND / NA)                  ' [V]
      PDD = P0 * (1 + NDD / NA)                ' [V]
      PM = P0 * k * F * l / Xj                 '~[V]
      P2 = PM * (L1 - LsatP) / l               '~[V]
      P3 = PM * L1 / l                         '~[V]
                                               '~ changes with LsatP
      'Calculate E(Y)
      Y1 = (Y + LsatP) / l
      Y2 = (Y + L1) / l
      Y3 = Y / l
      Y4 = (Y - LN) / l
      FEofY = PA * SINH(Y1) + l * Esat * COSH(Y1)
      IF Y2 >= 0 THEN
       IF Xdp < Xj THEN                        '2 sub regions
        FEofY = FEofY + PM * (COSH(Y2) - 1)
       ELSE
        FEofY = FEofY + PM * (COSH(Y1) - 1) + P2 * SINH(Y1)
       END IF
      END IF
      IF Y3 >= 0 THEN
       FEofY = FEofY - PM * (COSH(Y3) - 1) - PD * SINH(Y3)
      END IF
      IF Y4 >= 0 THEN FEofY = FEofY - (PDD - PD) * SINH(Y4)
      EofY = FEofY / l
      END FUNCTION

'=============================================================================
      SUB FindIDlin (X)
      'Calculates the drain current in the linear region
'=============================================================================
      'X=ID
      IF VDS = 0 THEN X = 0: EXIT SUB
      XL = 0: XH = IDsat
      FL = FofID(XL): FH = FofID(XH)
      IF FL * FH >= 0 THEN
       PRINT "FindIDlin: ROOT MUST BE BRACKETED FOR BISECTION": EXIT SUB
      END IF
      IF FL < 0 THEN
```

```
        X = XL: DX = XH - XL
       ELSE
        X = XH: DX = XL - XH
       END IF
       FOR I% = 1 TO ITERmax%
         DX = DX / 2
         XMID = X + DX
         FMID = FofID(XMID)
         IF FMID <= 0 THEN X = XMID
         IF ABS(DX) < DIconvg OR FMID = 0 THEN EXIT SUB
       NEXT I%
       PRINT "FindIDlin: TOO MANY SECTIONS": EXIT SUB
       END SUB

'=============================================================================
       SUB FindIE (X, I%)
       'Calculates current IE injected across the source junction
'=============================================================================
       'X = IE
       XL = 0: XH = IDT + .002
       FL = FofIE(XL): FH = FofIE(XH)
       IF FL * FH >= 0 THEN
        PRINT "FindIE: ROOT MUST BE BRACKETED FOR BISECTION": EXIT SUB
       END IF
       IF FL < 0 THEN
        X = XL: DX = XH - XL
       ELSE
        X = XH: DX = XL - XH
       END IF
       FOR I% = 1 TO ITERmax%
         DX = DX / 2
         XMID = X + DX
         FMID = FofIE(XMID)
         IF FMID <= 0 THEN X = XMID
         IF ABS(DX) < DIconvg OR FMID = 0 THEN EXIT SUB
       NEXT I%
       PRINT "TOO MANY SECTIONS": EXIT SUB
       END SUB

'=============================================================================
       SUB FindLsat (X, I%)
'=============================================================================
       'X=Lsat
       XL = 0: XH = L0 / 2
       FL = FofLsat(XL): FH = FofLsat(XH)
       IF FL * FH >= 0 THEN
        PRINT "FindLsat: ROOT MUST BE BRACKETED FOR BISECTION": EXIT SUB
       END IF
       IF FL < 0 THEN
        X = XL: DX = XH - XL
       ELSE
        X = XH: DX = XL - XH
       END IF
       FOR I% = 1 TO ITERmax%
         DX = DX / 2
         XMID = X + DX
         FMID = FofLsat(XMID)
         IF FMID <= 0 THEN X = XMID
         IF ABS(DX) < DLconvg OR FMID = 0 THEN EXIT SUB
        NEXT I%
```

```
      PRINT "FindLsat: TOO MANY SECTIONS": EXIT SUB
      END SUB

'=============================================================================
      SUB FindVDsat (X, I%)
      'Calculates VDsat by solving IDsat1(VDsat)-IDsat2(VDsat)=0
'=============================================================================
      XL = (VG - VTH) / 3
      XH = VG - VTH
      IF FofVDsat(XL) * FofVDsat(XH) >= 0 THEN
      PRINT "FindVDsat: ROOT MUST BE BRACKETED FOR BISECTION": EXIT SUB
      END IF
      FOR I% = 1 TO ITERmax%
        X = (XL + XH) / 2
        IF FofVDsat(XL) * FofVDsat(X) < 0 THEN XH = X ELSE XL = X
        DX = XH - XL
        IF DX < DVconvg OR FofVDsat(X) = 0 THEN EXIT SUB
      NEXT I%
      PRINT "TOO MANY SECTIONS": EXIT SUB
      END SUB

'=============================================================================
      SUB FindYd (X, I%)
'=============================================================================
      'X=Yd
      XL = 0: XH = 1.1 * LN
      FL = GofYd(XL): FH = GofYd(XH)
      IF FL * FH >= 0 THEN
       PRINT "FindYd: ROOT MUST BE BRACKETED FOR BISECTION": EXIT SUB
      END IF
      IF FL < 0 THEN
       X = XL: DX = XH - XL
      ELSE
       X = XH: DX = XL - XH
      END IF
      FOR I% = 1 TO ITERmax%
        DX = DX / 2
        XMID = X + DX
        FMID = GofYd(XMID)
        IF FMID <= 0 THEN X = XMID
        IF ABS(DX) < DLconvg OR FMID = 0 THEN EXIT SUB
      NEXT I%
      PRINT "TOO MANY SECTIONS": EXIT SUB
      END SUB

'=============================================================================
      FUNCTION FofID (X)
'=============================================================================
      'X=ID
      VG = VGS - RS * X
      VD = VDS - 2 * RS * X
      IF VD = 0 THEN FofID = 0: EXIT FUNCTION
      FF = (VG - VFB - 2 * PHIF - VD / 2) * VD
      GG = (2 / 3) * FSC(VD) * LAMBDA * ((VD + PHIS0) ^ 1.5 - (PHIS0) ^ 1.5)
      KK = BETA0 * (FF - GG)
      FofID = X - KK / (1 + (THETAS / VD) * (FF + GG) + VD / (L0 * ECRITL))
      END FUNCTION

'=============================================================================
      FUNCTION FofIE (X)
```

```
'================================================================================
        'X=IE
        IH = (M - 1) * (ICH + ke * ALPHA0 * X)
        IB = IH - (1 - ALPHA0) * X
        VF = IB * RB - (X + ICH) * RS + VB
        IF VF > .65 THEN VF = .65
        FofIE = X - I0 * (EXP(VF / vt) - 1)
        END FUNCTION

'================================================================================
        FUNCTION FofLsat (LsatP)
'================================================================================
        'V(Yd) = VYd = VD-RD*ID
        CALL GetVEYd(Yd, LsatP, VYd, EYd)
        FofLsat = VofY(Yd, LsatP) - VYd
        END FUNCTION

'================================================================================
        FUNCTION FofVDsat (X)
'================================================================================
        'X=VDsat
        FofVDsat = IDsat1(X) - IDsat2(X)
        END FUNCTION

'================================================================================
        FUNCTION FSC (X)
'================================================================================
        'X = VD
        VBI = vt * LOG(NA * ND / ni ^ 2)          ' [V]  built-in potential
        XS = ALPHA * SQR(PHIS(IB))                ' dep. width of the source junc.
        XD = ALPHA * SQR(PHIS(IB) + X)            ' dep. width of the drain junc.
        FXS = Xj / L0 * (SQR(1 + 2 * XS / Xj) - 1)
        FXD = Xj / L0 * (SQR(1 + 2 * XD / Xj) - 1)
        FSC = 1 - (FXS + FXD) / 2                 ' short channel factor
        END FUNCTION

'================================================================================
        SUB GetEsat
'       Solve for VDsat; Calculate Esat, IDsat
'================================================================================
        CALL FindVDsat(VDsat, ITERV%)
        VGP = VG - VFB - 2 * PHIF
        FAC = NN / (1 - NN) * ECRITL
        VBB = FSC(VDsat) * LAMBDA * SQR(VDsat + PHIS(IB))
        Esat = FAC * (1 + THETAS * (VGP + VBB - VDsat))
        IDsat = IDsat2(VDsat)
        END SUB

'================================================================================
        SUB GetIDT3
'       Calculate IDT and IB in the saturation-breakdown region
'================================================================================
        CALL FindIE(IE, ITERI%)                   'Calculate IE,IB,VF
        CALL GetEsat                              'Get new Esat, IDsat taking into
                                                  'account backgate bias IB*RB

        ICH = IDsat / (1 - Lsat / L0)
        IH = (M - 1) * (ICH + ke * ALPHA0 * IE)
        IB = IH - (1 - ALPHA0) * IE
        IDT = M * (ICH + ke * ALPHA0 * IE) + ALPHA0 * (1 - ke) * IE
        END SUB
```

```
'=============================================================================
      SUB GetLsat
      'Calculate location of the pinch-off point Lsat
'=============================================================================
      Yd = LN / 2                        'First guess for Yd; assume partial
                                         'depletion of LDD region
      Lsat = L0 / 2
      ITERtot% = 0
      YCNT% = 0
      LCNT% = 0
      DO
        ITERtot% = ITERtot% + 1
        LsatOld = Lsat
        YdOld = Yd
        'Solve for Lsat using V(Yd)=VD
        CALL FindLsat(Lsat, ITERL%)
        LCNT% = LCNT% + ITERL%
        'Solve for Yd using Ey(X=0,Yd) = 0
        CALL FindYd(Yd, ITERY%)
        YCNT% = YCNT% + ITERY%
        DELTA = ABS(Lsat - LsatOld) + ABS(Yd - YdOld)
      LOOP UNTIL (DELTA < DLconvg) OR (ITERtot% > ITERmaxTot%)
      END SUB

'=============================================================================
      SUB GetMfactor
      'Calculates maximum lateral electric field Emax and the
      'avalanche multiplication factor M
'=============================================================================
      DY = (Yd + Lsat) / 100
      S = 0
      FOR Y = (-Lsat + DY / 2) TO Yd STEP DY
        E = EofY(Y, Lsat)
        S = S + EXP(-Bi / E)
      NEXT Y
      S = Ai * S * DY
      M = 1 / (1 - S)
      END SUB

'=============================================================================
      SUB GetVEYd (YdP, LsatP, VYd, EYd)
'=============================================================================
      I = IDsat / (1 - LsatP / L0)           'Channel length modulation
      ID = (I + ke * ALPHA0 * IE) * M        'Including IE and multiplication
      RL = RHO * LN / (W * Xj)               '[OHM] resistance of LDD region
      IF YdP > 0 AND YdP < LN THEN           'Yd in LDD region
       RD = RHO * (LN - YdP) / (W * Xj)      '[OHM] res. of the undepleted LDD
       VYd = VDS - ID * (2 * RS - (RL - RD)) 'V(Yd)
       EYd = ID * RD / (LN - YdP)            'E(X=0,Yd)
      ELSEIF YdP <= 0 THEN                   'YD in sub region ?
       VYd = VDS - ID * 2 * RS               'V(Yd)
       EYd = ID * RL / LN                    'E(X=0,Yd)
      ELSE                                   'Yd in HDD region
       RD = 0                                '[OHM]
       VYd = VDS - ID * (2 * RS - RL)        'V(Yd)
       EYd = 0                               'E(X=0,Yd)
      END IF
      END SUB
```

```
'=============================================================================
      SUB GetVF
'     Calculate Forward bias voltage.
'=============================================================================
      CALL GetEsat
      ICH = IDsat / (1 - Lsat / L0)
      IB = (M - 1) * ICH
      VF = IB * RB - ICH * RS + VB
      END SUB

'=============================================================================
      FUNCTION GofYd (YdP)
      'E(Yd)=EYd=(VD-VYd)/(LN-Yd)
'=============================================================================
      CALL GetVEYd(YdP, Lsat, VYd, EYd)
      GofYd = EofY(YdP, Lsat) - EYd
      END FUNCTION

'=============================================================================
      FUNCTION IDsat1 (X)
'=============================================================================
      'X=VDsat
      VGP = VG - VFB - 2 * PHIF
      FAC = NN * BETA0 * L0 * ECRITL
      IDsat1 = FAC * (VGP - LAMBDA * FSC(X) * SQR(X + PHIS(IB)) - X)
      END FUNCTION

'=============================================================================
      FUNCTION IDsat2 (X)
'=============================================================================
      'X=VDsat
      IF X = 0 THEN IDsat2 = 0: EXIT FUNCTION
      FF = (VG - VFB - 2 * PHIF - X / 2) * X
   GG = (2 / 3) * FSC(X) * LAMBDA * ((X + PHIS(IB)) ^ 1.5 - (PHIS(IB)) ^ 1.5)
      KK = BETA0 * (FF - GG)
      IDsat2 = KK / (1 + (THETAS / X) * (FF + GG) + X / (L0 * ECRITL))
      END FUNCTION

'=============================================================================
      FUNCTION PHIS (IB)
'=============================================================================
      PHI = 2 * PHIF - VB - IB * RB
      IF PHI < 0 THEN PHI = 0
      PHIS = PHI
      END FUNCTION

'=============================================================================
      FUNCTION SINH (X)
'=============================================================================
      E = EXP(X)
      SINH = (E - 1 / E) / 2
      END FUNCTION

'=============================================================================
      FUNCTION VofY (Y, LsatP)
'=============================================================================
      Xdp = ALPHA * SQR(PHIS(IB) + VDsat)      'Dep. region edge at the
                                               'pinch-off point
      Xdd = ALPHA * SQR(PHIS(IB) + VD) + Xjd   'Dep. region edge at HDD
      l = SQR(Xj * esi / COX)                  '[cm] characteristic length
```

```
k = (Xdd - Xdp) / (LsatP + LN)          '~Slope of depletion width edge
L1 = LsatP + (Xdp - Xj) / k             '~[cm] Y @ dep. width=Xj
P0 = qe * NA * Xj / COX                 ' [V]
PA = P0 * (1 - (Xdp / Xj) * FSC(VD))    '[V]
PD = P0 * (1 + ND / NA)                 ' [V]
PDD = P0 * (1 + NDD / NA)               ' [V]
PM = P0 * k * F * l / Xj                '~[V]
P2 = PM * (L1 - LsatP) / l              '~[V]
P3 = PM * L1 / l                        '~[V]
                                        '~ changes with LsatP

'Calculate V(Y)
Y1 = (Y + LsatP) / l
Y2 = (Y + L1) / l
Y3 = Y / l
Y4 = (Y - LN) / l
FVofY = PA * COSH(Y1) + l * Esat * SINH(Y1)
IF Y2 >= 0 THEN
 IF Xdp < Xj THEN
  FVofY = FVofY + PM * (SINH(Y2) - Y2)      '2 Sub regions
 ELSE
  FVofY = FVofY + PM * (SINH(Y1) - Y1) + P2 * (COSH(Y1) - 1)
 END IF
END IF
IF Y3 >= 0 THEN
 FVofY = FVofY - PM * (SINH(Y3) - Y3) - PD * (COSH(Y3) - 1)
END IF
IF Y4 >= 0 THEN
 FVofY = FVofY - (PDD - PD) * (COSH(Y4) - 1)
END IF
VofY = FVofY + VDsat - PA
END FUNCTION

'=============================================================================
SUB WritePars
'=============================================================================
 LPRINT "     TRANSISTOR PARAMETERS AND OPERATING CONDITIONS:"
 LPRINT ""
 LPRINT "     VDSstep       [V]          "; VDSstep
 LPRINT "     VGS           [V]          "; VGS
 LPRINT "     VBS           [V]          "; VBS
 LPRINT "     L0            [um]         "; L0 * 10000!
 LPRINT "     NA            [cm^-3]      "; NA
 LPRINT "     ND            [cm^-3]      "; ND
 LPRINT "     NDD           [cm^-3]      "; NDD
 LPRINT "     Xj            [um]         "; Xj * 10000!
 LPRINT "     Xjd           [um]         "; Xjd * 10000!
 LPRINT "     Ln            [um]         "; LN * 10000!
 LPRINT "     F (fringing factor)        "; F
 LPRINT "     n (saturation level)       "; NN
 LPRINT "     VFB           [V]          "; VFB
 LPRINT "     EcritL        [MV/cm]      "; ECRITL * .000001
 LPRINT "     EcritN        [MV/cm]      "; ECRITN * .000001
 LPRINT "     U0            [cm^2/V-s]   "; U0
 LPRINT "     UD            [cm^2/V-s]   "; UD
 LPRINT "     COX           [F/cm^2]     "; COX
 LPRINT "     LAMBDA        [V^.5]       "; LAMBDA
 LPRINT "     ALPHA         [cm/V^.5]    "; ALPHA
 LPRINT "     PHIF          [V]          "; PHIF
 LPRINT "     PHIS0         [V]          "; PHIS0
 LPRINT "     BETA0         [A/V^2]      "; BETA0
```

```
 LPRINT "      VTH             [V]             "; VTH
 LPRINT "      THETAS          [1/V]           "; THETAS
 LPRINT "      RHO             [ohm-cm]        "; RHO
 LPRINT "      RB              [ohm]           "; RB
 LPRINT "      RS              [ohm]           "; RS
 LPRINT "      I0              [A]             "; I0
 LPRINT ""
 LPRINT "      SIMULATION PARAMETERS:"
 LPRINT ""
 LPRINT "      dV (convg)      [V]             "; DVconvg
 LPRINT "      dL (convg)      [cm]            "; DLconvg
 LPRINT "      dI (convg)      [A]             "; DIconvg
 LPRINT "      Max # of iterations             "
 LPRINT "      for VDsat, Lsat, Yd, IE         "; ITERmax%
 LPRINT "      Max total iter. for Lsat        "; ITERmaxTot%
END SUB
```

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Vita

Zbigniew A. Kozlowski was born in Warsaw, Poland on February 3, 1948. He is the son of Halina and Czeslaw Kozlowski. He received the B.S. degree in Electrical Engineering from Warsaw Polytechnic in December of 1971. From 1972 to 1977 he worked on image intensifiers at the Institute of Electron Technology in Warsaw, Poland. From 1977 to 1981 he worked as a process engineer for UNITRA-POLKOLOR in Piaseczno, Poland, a manufacturer of color TV picure tubes. Since 1983 he has been working with AT&T Microelectronics in Allentown, Pa. He currently is a process technologist for Flash EEPROMs.

END

OF

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